Claims

1. A pulse width modulator circuit for generating a reference signal having a desired duty cycle comprising
   an adjustment unit including at least one storage register and a counter, the storage register being configured for storing values corresponding to the desired duty cycle at least approximately and which are set during a working cycle in the pulse width modulator circuit for generating a reference signal, and the counter setting a cycle count (Y) indicating how often a stored first value (X) is read during the working cycle (A) from the storage register, the value stored in the storage register being variable during the working cycle.

2. The pulse width modulator circuit as set forth in claim 1, comprising an adder which receives the stored first value from the storage register and changes it upon reaching the cycle count (Y) to generate a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is reached.

3. The pulse width modulator circuit as set forth in claim 1, wherein the first value stored in the storage register is variable upon reaching the cycle count (Y) to store a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is reached.

4. The pulse width modulator circuit as set forth in claim 1, 2 or 3 wherein the storage register has an 8 bit capacity and the counter a 3 bit capacity.

5. A power supply including
   switching means (20) and
   a pulse width modulator circuit (34) as set forth in any of the preceding claims for outputting to the switching means (20) a control signal having a desired duty cycle and corresponding to the reference signal.

6. A method for driving a pulse width modulator circuit comprising the steps:

- generating a pulse width control signal having a desired duty cycle,
- defining at least one first value and a second value (46, 48) corresponding at least approximately to the desired duty cycle and being output during a working cycle for generating the pulse width control signal A times in all, where A is a predefined number, and
- setting (44) a cycle count Y dictating how often the first value and how often the second value is read during the working cycle to set the desired duty cycle as a function of an average of the first and second values output during the working cycle.

7. The method as set forth in claim 6 wherein the first value and the second value are output to a pulse width modulator (34) for generating the pulse width control signal.

8. The method as set forth in claim 6 or 7 wherein a first value is output Y times and the second value is output (A-Y) times.

9. The method as set forth in any of the claims 6 to 8 wherein the first value is an integer X and the second value is an integer X+1.

10. The method as set forth in claim 9 wherein the first value is stored in a storage register and the second value (X+1) is generated by the addition of 1 to the first value.

11. The method as set forth in any of the claims 6 to 10 wherein the cycle count Y is set in a counter, the first value is output (46) during each count clock until the cycle count Y is reached and the second value is output (48) during each count clock after the cycle count is reached up to the end of the working cycle A.

12. The method as set forth in claim 11 wherein the counter is reset at the end of each working cycle (52).

13. A method for driving a power supply wherein a pulse width control signal is generated as set forth in any of the claims 6 to 12 and is applied to switching means (20) for generating an output current.

14. A computer program comprising a program code for implementing the method as set forth in any of the claims 6 to 13.